Three Phases BLDC Motor Controller

1. Overview

1.1. General Description

The EMT1042 integrates the 8051 core with peripheral circuits to perform sine-wave motor control. For rotor position detection, it can support sensorless motor or Hall latch IC input. In addition, system level peripheral functions, such as ADC, OPAMP, Comparator, communication interface, SVPWM, watchdog timer, current sensing, undervoltage-lockout (UVLO), over current protection (OCP) and locked-rotor protection are integrated to reduce component count, PCB size and system cost.

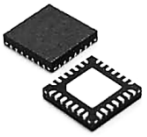
1.2. Features

- Operation Frequency 24MHz
- High-performance 8051 Microcontroller
- Vector Interrupt Controller, 12 Interrupt Sources
- Operating Voltage Range: 4.5V to 5.5V
- Memory size :
  - 32KB Flash Program Memory
  - 256 x 8bit IRAM
  - 4K x 8bit XRAM
- Up to 19 General-Purpose Input / Output(GPIO) Pins
- Two Timers
- Watchdog (WD) Timer
- 8 Channels 12-bit ADC Converter
- 1 UART Serial Channel
  - Support CRC-8
  - 40 bytes Transmit and Receive Data Buffers
- 16-bit PWM generator with Dead Time Control
- 16-bit PWM_DAC generator
- MDU：Signed/unsigned 32x32、16x16、32/16、16/16
- Code Protection for Flash
- Deep Sleep Mode Current Less than 200uA
- Support
  - Sensorless + 1 or 3 shunts
  - 3 Hall ICs + 1 or 3 shunts
  - 1 Hall IC + 1 shunt
- Space Vector PWM (SVPWM)
- Current Phase Compensator
- Initial Position Detection (IPD)
- Built in 3 OPAs (PGA, Max gain:20)
- Built in 5 Comparators (with 4-channel Ref. Max 1.0V)
- ADC0~5 Support Auto Convert
- 1 Channel 12-bit PWMIN
- 1 Channel Capture
- Protections: OCP, OVP, UVLO, Lock Protection and Phase Unconnected Protection

1.3. Package Type

TSSOP-28L

TQFN4x4-28L

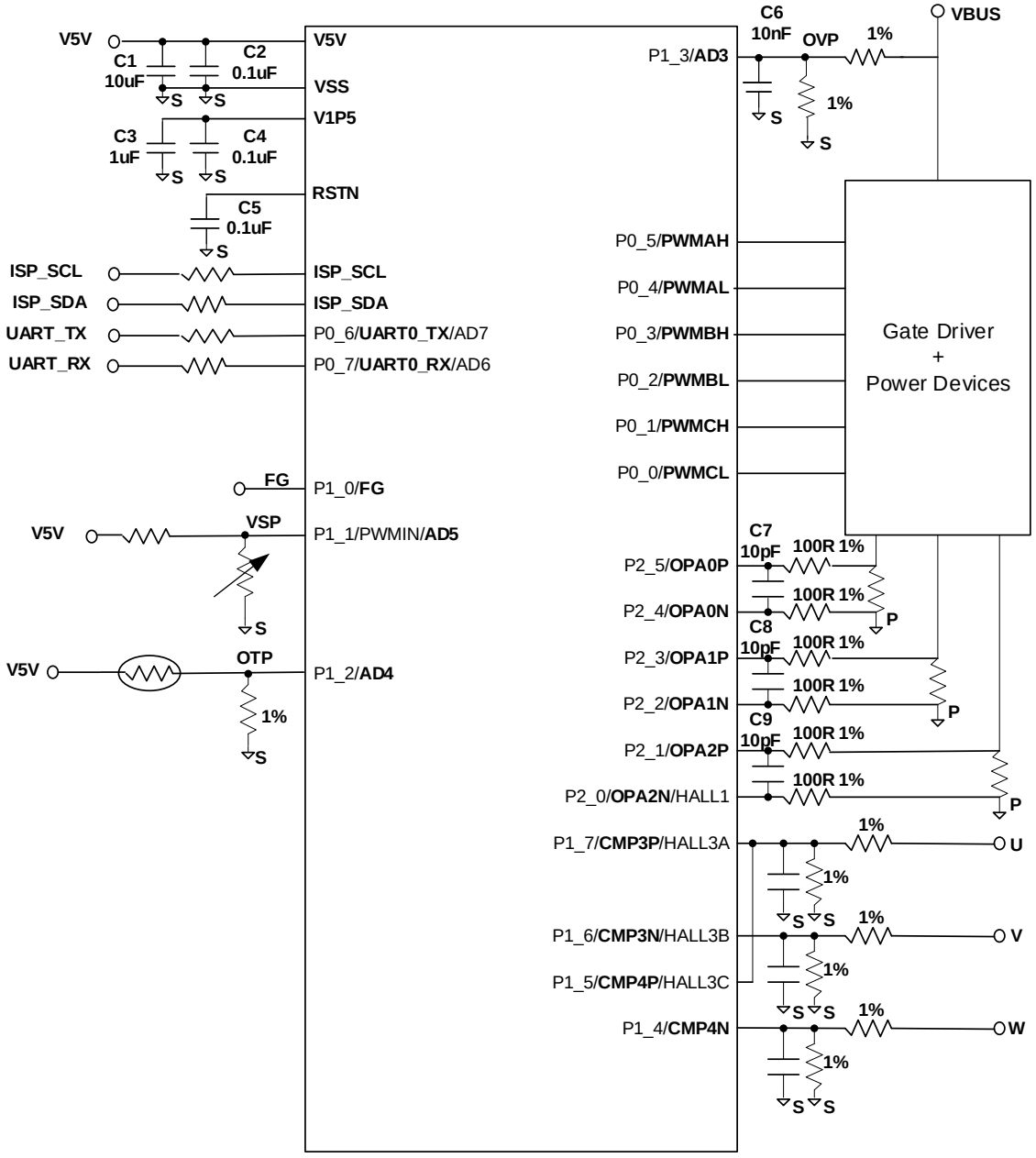


1.4. Applications

- 3 phases BLDC fan motor
- Pedestal fan
- Ventilation fan
- Exhaust fan
- Air cleaner
- Humidifiers
- Range hood

1.5. Typical Application Circuit

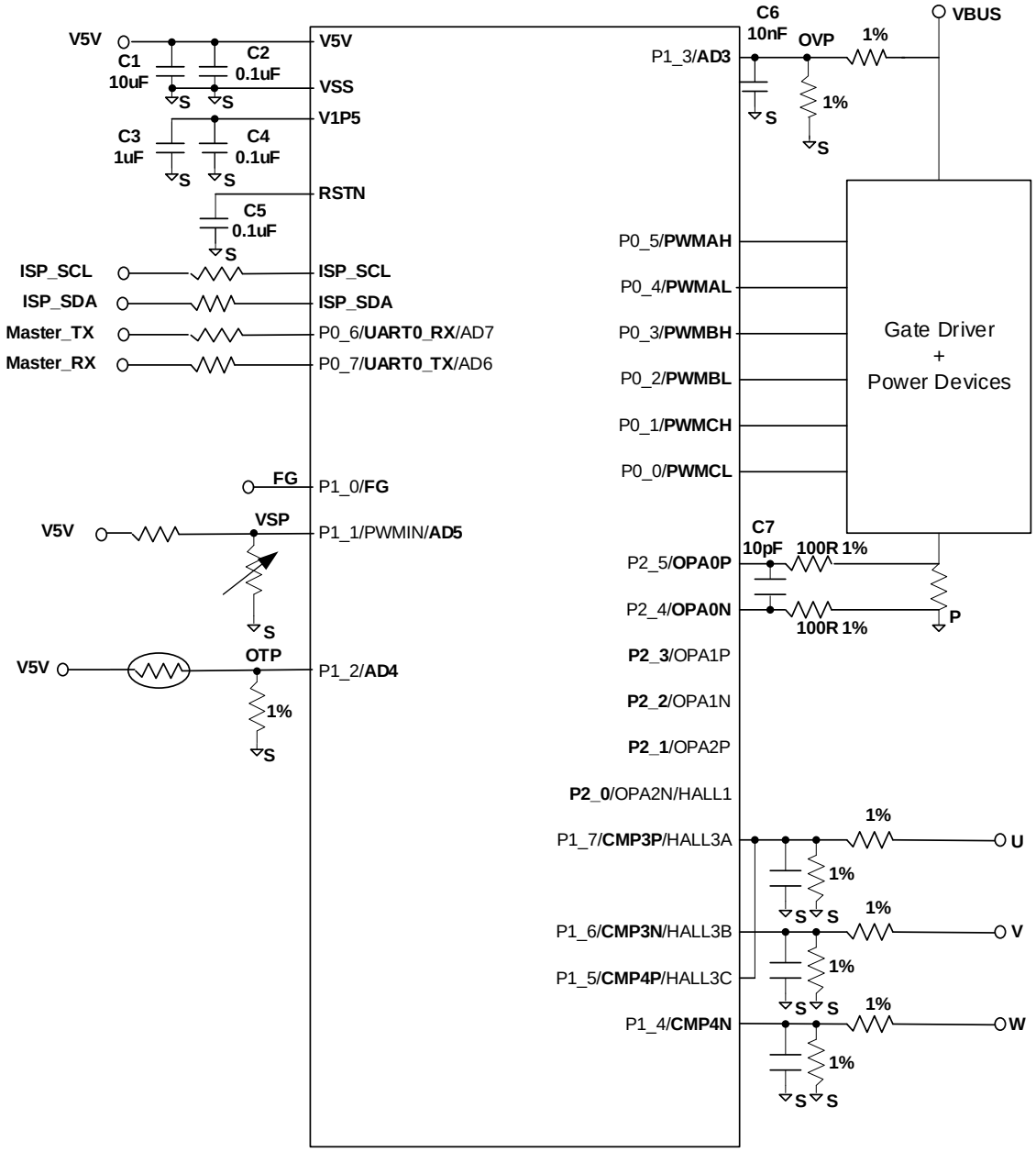
Sensorless + 3 Shunts



Note:

1. C1, C2, C3, C4, and C5 shall be placed as close to the controller as possible.
2. Value 1nF ~ 10nF is recommended for C6.
3. C7 to C9 and six 100R resistors shall be placed as close to the controller as possible.
4. Current sensing wirings shall be differential pairs for each phase from the shunt resistor to the controller.
5. Value 10pF ~ 1nF is recommended for C7 to C9.
6. The Power ground(P) and Signal ground(S) are connected by a single point.

Sensorless + 1 Shunt



Note:

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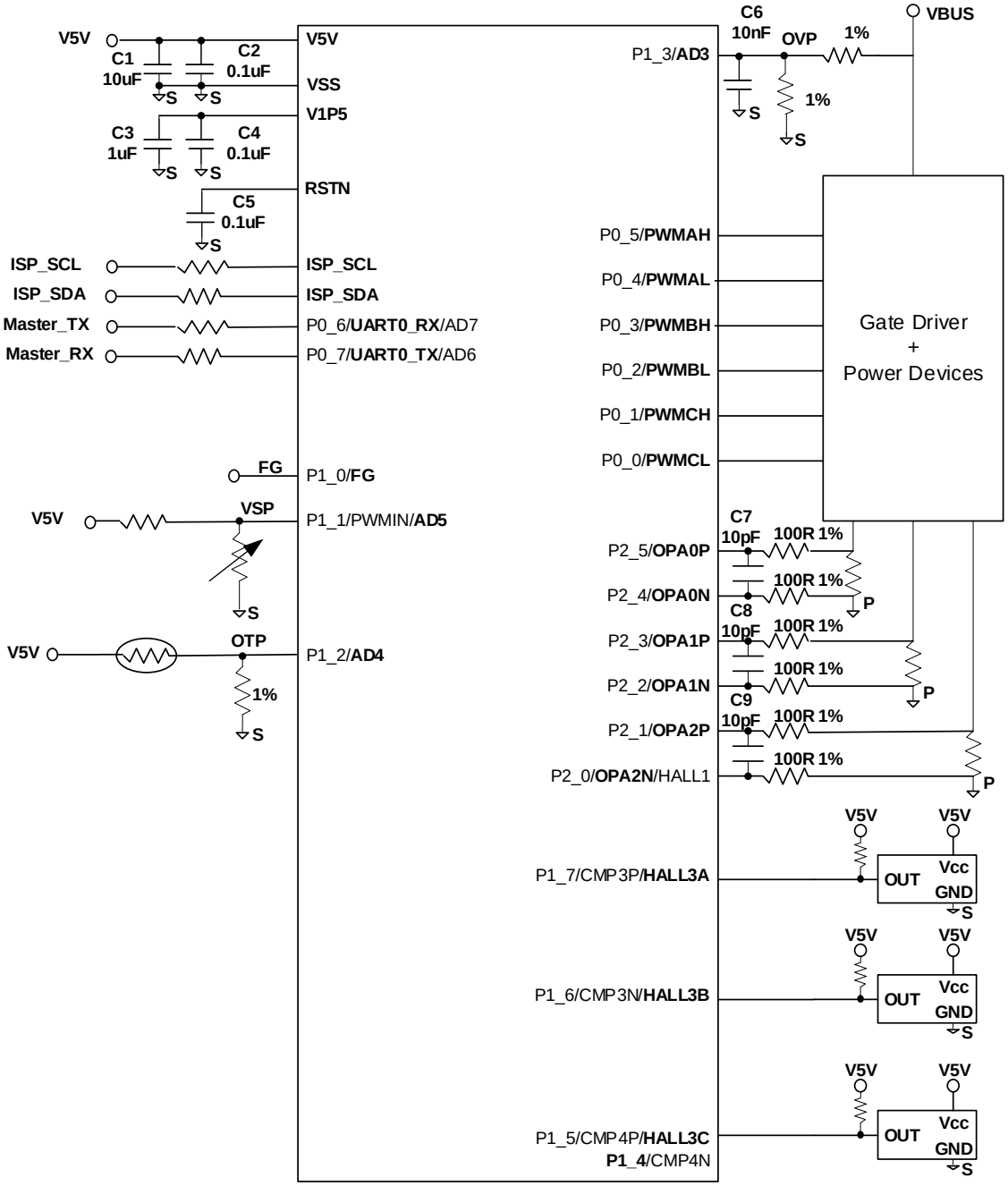
2. Value 1nF ~ 10nF is recommended for C6.
3. C7 and two 100R resistors shall be placed as close to the controller as possible.
4. Current sensing wirings shall be differential pairs for each phase from the shunt resistor to the controller.
5. Value 10pF ~ 1nF is recommended for C7.
6. The Power ground(P) and Signal ground(S) are connected by a single point.

3 Hall ICs + 3 shunts



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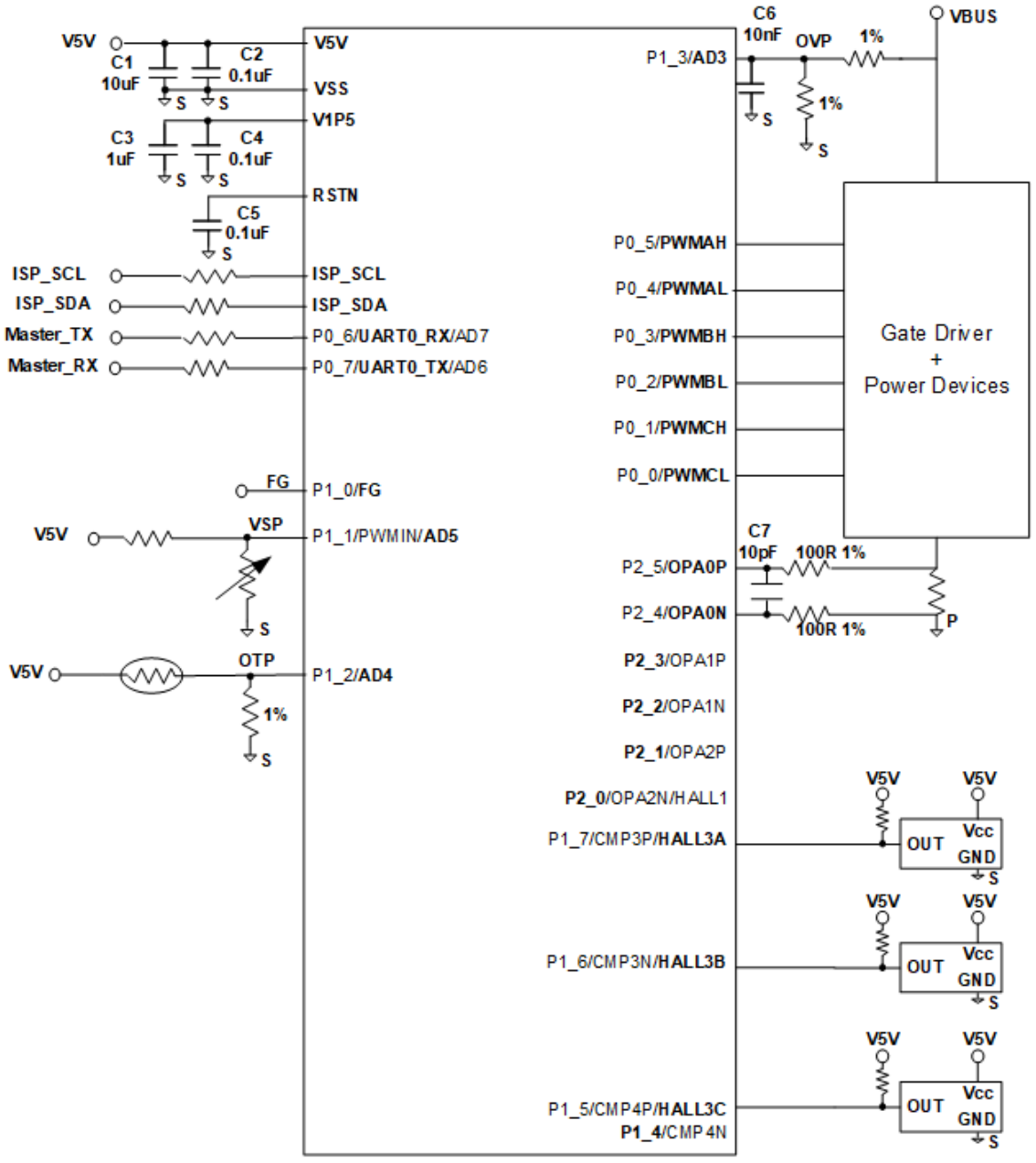
6. The Power ground(P) and Signal ground(S) are connected by a single point.

3 Hall ICs + 1 shunt



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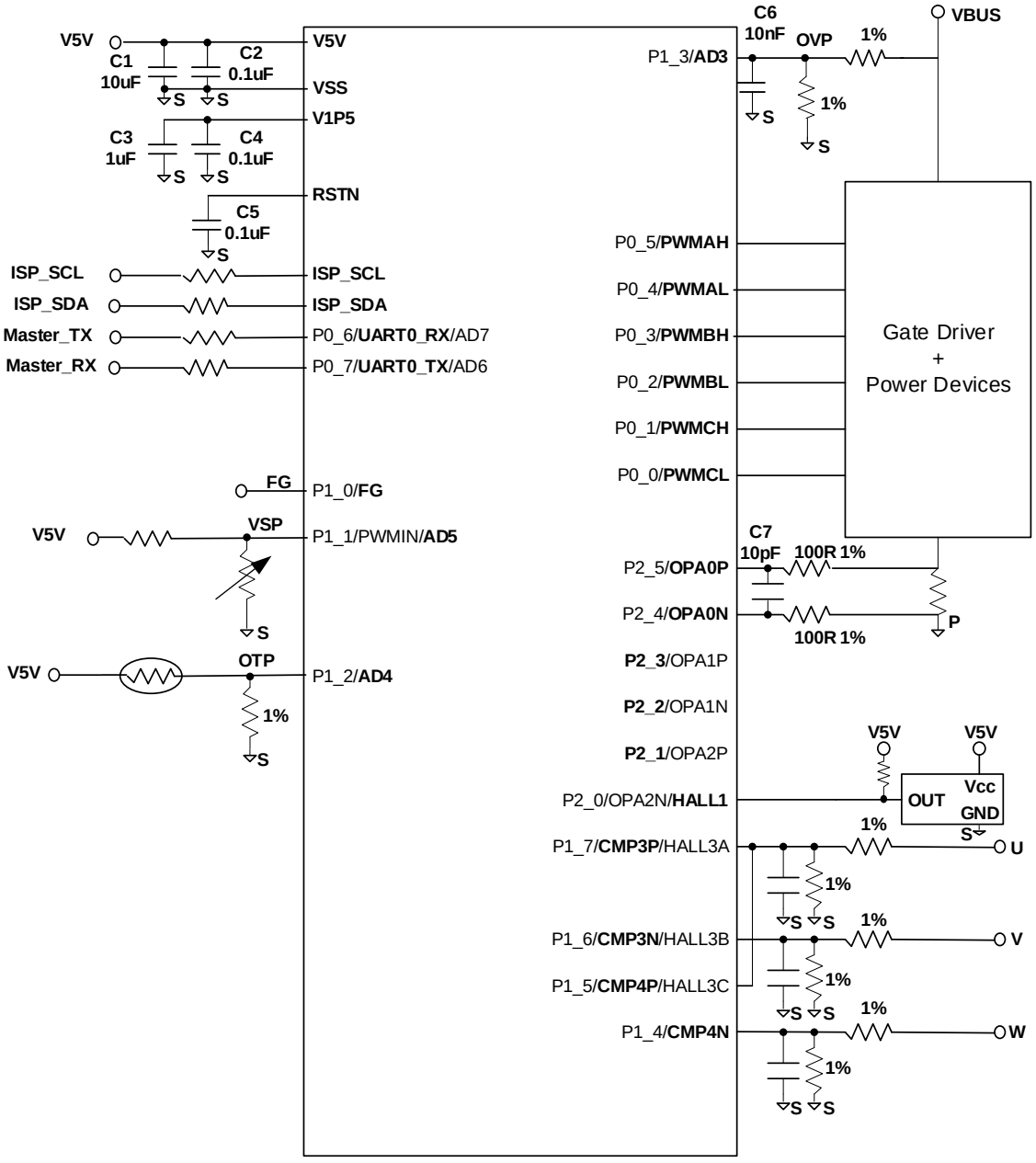
5. Value 10pF ~ 1nF is recommended for C7.
6. The Power ground(P) and Signal ground(S) are connected by a single point.

1 Hall IC + 1 shunt



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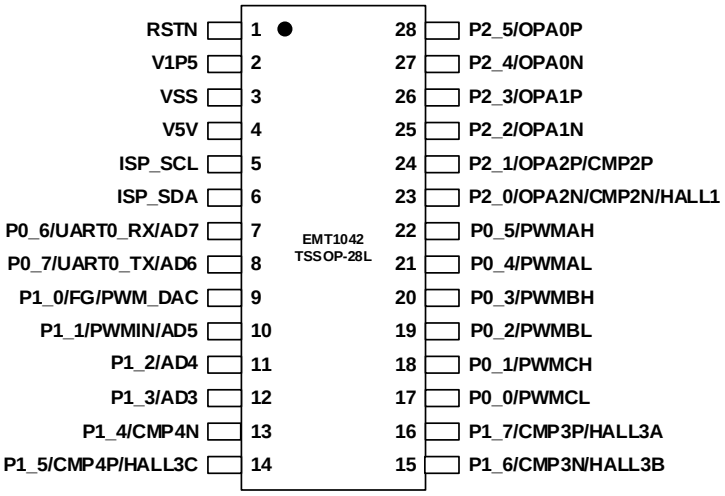
6. The Power ground(P) and Signal ground(S) are connected by a single point.

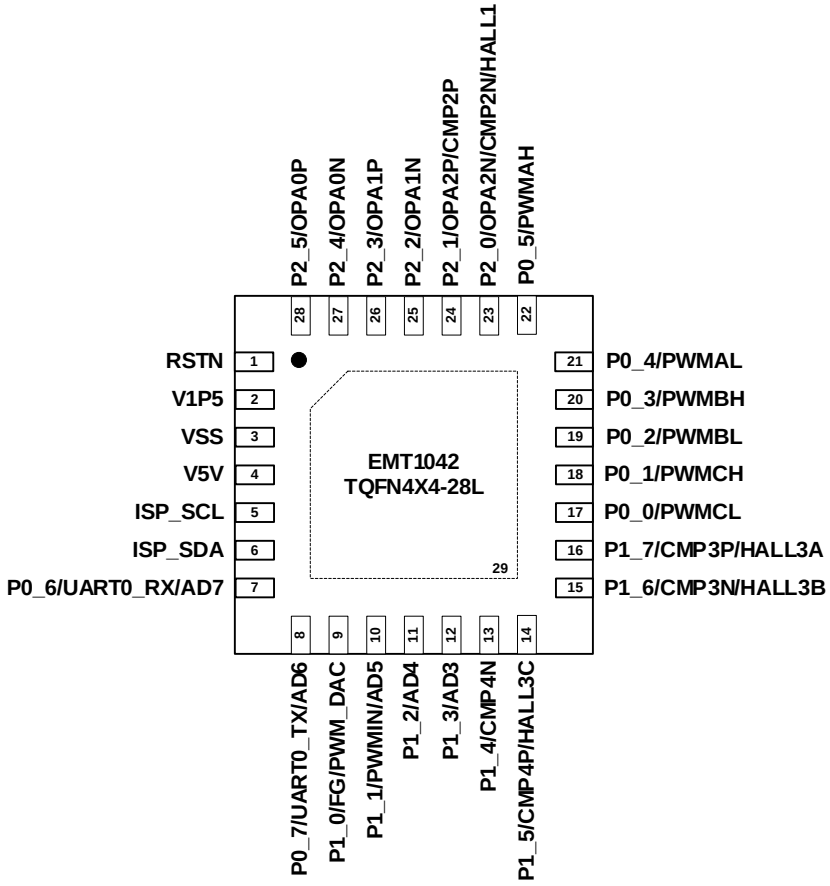
1.6. Pinouts and pin description

[TSSOP-28L]



Top View

[TQFN4x4-28L]



Top View

1.7. Functional Pin Description

Pin	Name	Type	Pin Function
1	RSTN	DI	Low active reset pin.
2	V1P5	PO	Core power LDO 1.5V output pin. (for core use only)
3	VSS	GND	Ground.
4	V5V	PI	5V power input pin.
5	ISP_SCL	DI	ISP clock pin.
6	ISP_SDA	DIO	ISP data pin.
7	P0_6	DIO	Pin 6 of GPIO port 0.
	UART0_RX	DO	UART0 receiving pin.
	AD7	AI	ADC Channel 7 input pin.
8	P0_7	DIO	Pin 7 of GPIO port 0.
	UART0_TX	DI	UART0 transmitting pin.
	AD6	AI	ADC Channel 6 input pin.
9	P1_0	DIO	Pin 0 of GPIO port 1.
	FG	DO	FG signal output pin. [Special support as UART0 transmitting pin]
	PWM_DAC	DO	PWM_DAC signal output pin
10	P1_1	DIO	Pin 1 of GPIO port 1.
	PWMIN	DI	PWM signal input pin. [Special support as UART0 receiving pin]
	AD5	AI	ADC Channel 5 input pin.
11	P1_2	DIO	Pin 2 of GPIO port 1.
	AD4	AI	ADC Channel 4 input pin.
12	P1_3	DIO	Pin 3 of GPIO port 1.
	AD3	AI	ADC Channel 3 input pin.
13	P1_4	DIO	Pin 4 of GPIO port 1.
	CMP4N	AI	CMP4 N input pin
14	P1_5	DIO	Pin 5 of GPIO port 1.

	CMP4P	AI	CMP4 P input pin
	HALL3C	DI	HALL C input pin(3 HALL MODE)
15	P1_6	DIO	Pin 6 of GPIO port 1.
	CMP3N	AI	CMP3 N input pin
	HALL3B	DI	HALL B input pin(3 HALL MODE)
16	P1_7	DIO	Pin 7 of GPIO port 1.
	CMP3P	AI	CMP3 P input pin
	HALL3A	DI	HALL A input pin(3 HALL MODE)
17	P0_0	DIO	Pin 0 of GPIO port 0.
	PWMCL	DO	PWM output, low side gate driver signal of phase C.
18	P0_1	DIO	Pin 1 of GPIO port 0.
	PWMCH	DO	PWM output, high side gate driver signal of phase C.
19	P0_2	DIO	Pin 2 of GPIO port 0.
	PWMBL	DO	PWM output, low side gate driver signal of phase B.
20	P0_3	DIO	Pin 3 of GPIO port 0.
	PWMBH	DO	PWM output, high side gate driver signal of phase B.
21	P0_4	DIO	Pin 4 of GPIO port 0.
	PWMAL	DO	PWM output, low side gate driver signal of phase A.
22	P0_5	DIO	Pin 5 of GPIO port 0.
	PWMAH	DO	PWM output, high side gate driver signal of phase A.
23	P2_0	DIO	Pin 0 of GPIO port 2
	OPA2N	AI	OPA2 N input pin
	CMP2N	AI	CMP2 N input pin
	HALL1	DI	HALL input pin(1 HALL MODE)
24	P2_1	DI	Pin 1 of GPI port 2. (only input)
	OPA2P	AI	OPA2 & CMP2 P- input pin
	CMP2P	AI	CMP3 P input pin

25	P2_2	DIO	Pin 2 of GPIO port 2.
	OPA1N	AI	OPA1 N- input pin
26	P2_3	DI	Pin 3 of GPI port 2. (only input)
	OPA1P	AI	OPA1 & CMP1 P- input pin
27	P2_4	DIO	Pin 4 of GPIO port 2
	OPA0N	AI	OPA0 N- input pin
28	P2_5	DI	Pin 5 of GPI port 2. (only input)
	OPA0P	AI	OPA0 & CMP0 P- input pin
29	Exposed Pad	GND	Connected to Ground. [Only for TQFN]

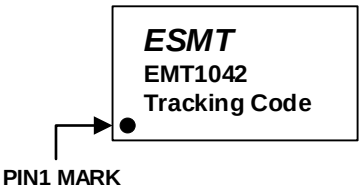
IO Type Definition :
DIO : Digital input/output pin.
DI : Digital input pin.
DO : Digital output pin.
AI : Analog input pin.
PI : Power Input pin.
PO : Power output pin.

1.8. Ordering Information

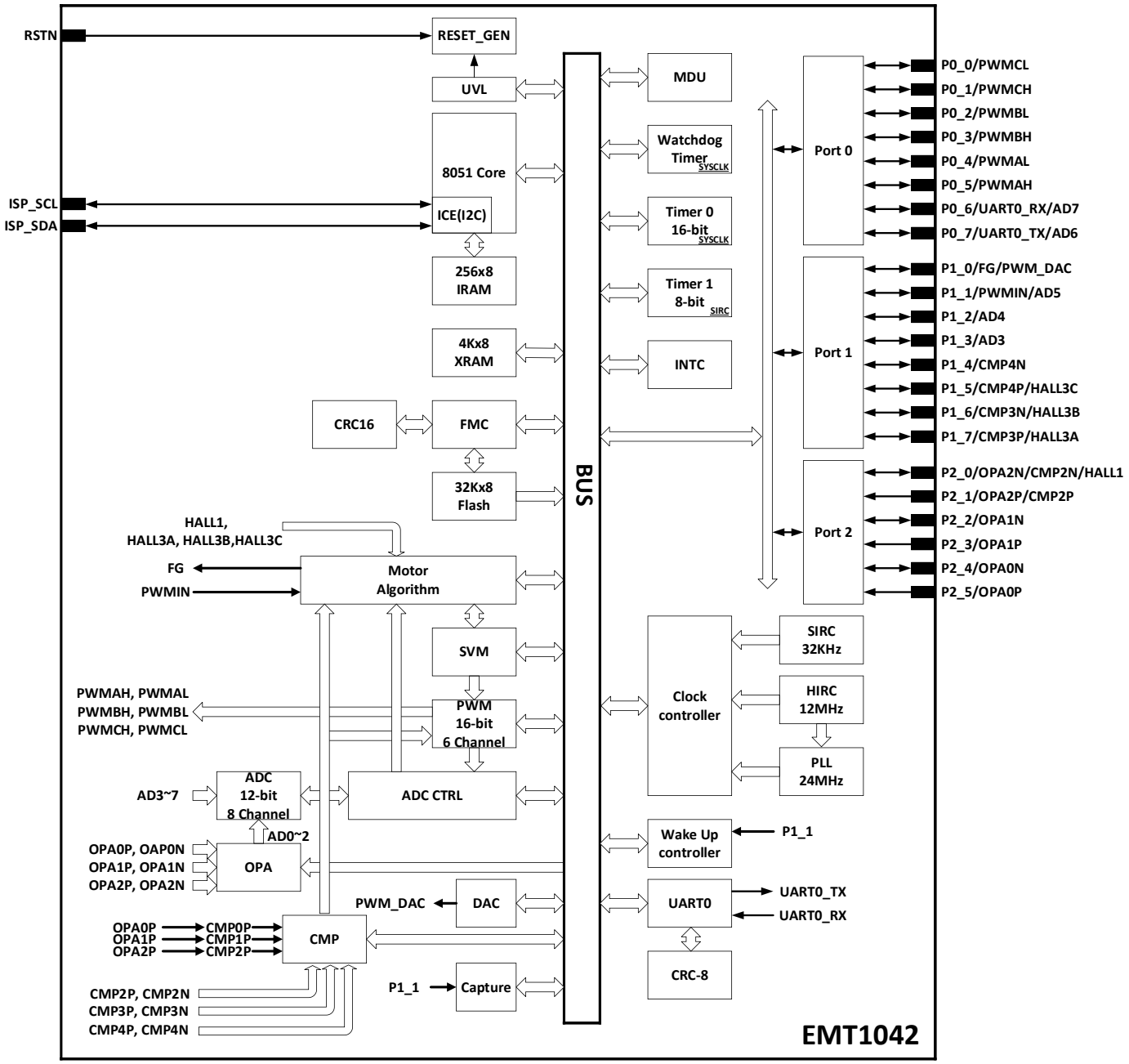
Product ID	Package Type	Packing / MPQ	Comments
EMT1042-TS28NBR	TSSOP-28L	2500 Units / Reel 2500 Units / Small Box	Green
EMT1042-NC28NBR	TQFN4x4-28L	3000 Units / Reel 6000 Units / Small Box	Green

1.9. Marking Information

EMT1042
Line 1 : LOGO
Line 2 : Product No.
Line 3 : Tracking Code



1.10. EMT1042 Block Diagram



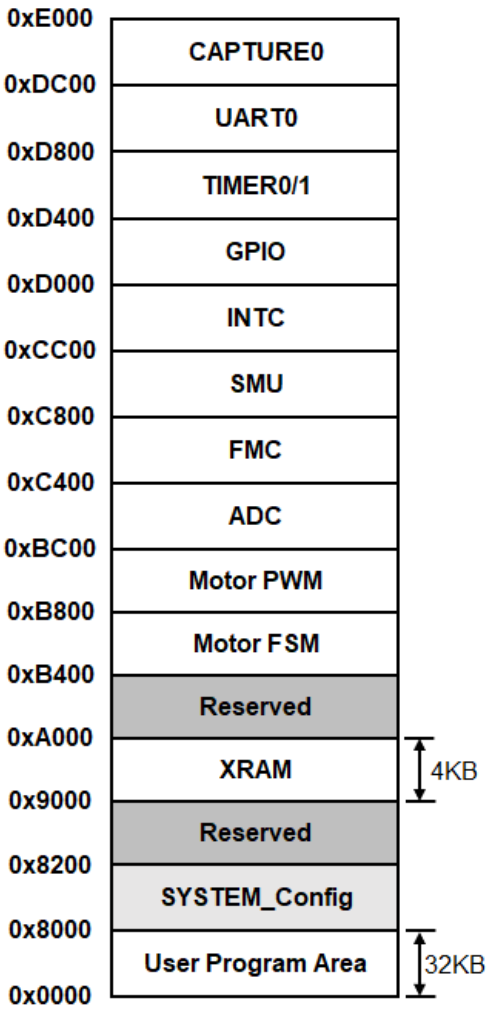
1.11. Memory Map

SFRs Memory Map:

F8H	MD_CTRL				MD4	MD5	MD6	MD7	FFH
F0H	B				MD0	MD1	MD2	MD3	F7H
E8H		RX_DATA_35	RX_DATA_36	RX_DATA_37	RX_DATA_38	RX_DATA_39			EFH
E0H	ACC	RX_DATA_28	RX_DATA_29	RX_DATA_30	RX_DATA_31	RX_DATA_32	RX_DATA_33	RX_DATA_34	E7H
D8H		RX_DATA_21	RX_DATA_22	RX_DATA_23	RX_DATA_24	RX_DATA_25	RX_DATA_26	RX_DATA_27	DFH
D0H	PSW	RX_DATA_14	RX_DATA_15	RX_DATA_16	RX_DATA_17	RX_DATA_18	RX_DATA_19	RX_DATA_20	D7H
C8H		RX_DATA_7	RX_DATA_8	RX_DATA_9	RX_DATA_10	RX_DATA_11	RX_DATA_12	RX_DATA_13	CFH
C0H		RX_ATA_0	RX_DATA_1	RX_DATA_2	RX_DATA_3	RX_DATA_4	RX_DATA_5	RX_DATA_6	C7H
B8H		TX_DATA_35	TX_DATA_36	TX_DATA_37	TX_DATA_38	TX_DATA_39			BFH
B0H		TX_DATA_28	TX_DATA_29	TX_DATA_30	TX_DATA_31	TX_DATA_32	TX_DATA_33	TX_DATA_34	B7H
A8H		TX_DATA_21	TX_DATA_22	TX_DATA_23	TX_DATA_24	TX_DATA_25	TX_DATA_26	TX_DATA_27	AFH
A0H	P2	TX_DATA_14	TX_DATA_15	TX_DATA_16	TX_DATA_17	TX_DATA_18	TX_DATA_19	TX_DATA_20	A7H
98H		TX_DATA_7	TX_DATA_8	TX_DATA_9	TX_DATA_10	TX_DATA_11	TX_DATA_12	TX_DATA_13	9FH
90H	P1	TX_DATA_0	TX_DATA_1	TX_DATA_2	TX_DATA_3	TX_DATA_4	TX_DATA_5	TX_DATA_6	97H
88H							DPPL	DPPH	8FH
80H	P0	SP	DPL	DPH					87H

Note: No reserved for user define.

XSFRs Memory Map:



2. Electrical Specifications

2.1. Absolute Maximum Ratings (Note1,2)

Supply Input Voltage, V5V	-0.3V to +5.8V	Storage Temperature Range	-55°C to 150 °C
PAD P2_1, P2_3, P2_5	-1.2V to +5.8V	Junction Temperature (T_J)	150 °C
I/O Pins	-0.3V to 5.8V	ESD Rating (Note3)	
Lead Temperature (Soldering, 10 sec.)	260°C	Human Body Model	2KV

2.2. Recommended Operating Conditions (Note1,2)

Supply Input Voltage, V5V	4.5V to 5.5V	Minimum Time Period of RSTN	100μs
Input Capacitor on V5V	10μF+0.1uF	Junction Temperature Range	-40°C to 125 °C
LDO Output Capacitor on V1P5	1μF+0.1uF	Ambient Temperature Range	-40°C to 105 °C
Voltage of I/O and RSTN to GND	-0.3V to V_{V5V}+0.3V		
Analog Input Voltage	-0.3V to V_{V5V}+0.3V		

2.3. Electrical Characteristics

V_{V5V}=5V, T_A=25℃, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock Section						
System Frequency	f_{SYSCLK}		12	24	--	MHz
Internal RC Oscillator						
Internal High RC Oscillator	f_{HIRC}		11.76	12	12.24	MHz
Internal Slow RC Oscillator	f_{SIRC}		20	32	48	KHz
PLL Section						
PLL 24MHz Clock	f_{PLL24M}		23.52	24	24.48	MHz
Power Management Section						
Supply Input of V5V	V_{V5V}		4.5	5.0	5.5	V
Turn-On Voltage of V5V	V_{V5V_ON}	According to LVR or UVLO configuration, maximum between V_{LVR} and V_{UVLO}	--	V_{LVR} or V_{UVLO}	--	V
V5V On-Off Hysteresis **(Note5)**	V_{V5V_HYS}	Turn-off voltage = V_{V5V_ON} - V_{V5V_hys}	--	0.05	--	V
LVR **(Note4,5)**	V_{LVR}		Typ. -3%	2.8	Typ. +3%	V
UVLO Level (4 level select) **(Note5)**	V_{UVLO}	UVL_LEVEL: 00: 2.7V 01: 3.0V 10: 3.7V 11: 4.3V	Typ. -3%	- 2.7 3.0 3.7 4.3	Typ. +3%	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
V5V Current at Operation Mode	I_{V5V_OPER}	Typical sensorless motor control mode	--	18	--	mA
V5V Current at Deep Sleep Mode	I_{V5V_DSLP}		--	200	--	μA
Internal 1.5V LDO (for core use only)						
LDO Voltage for Internal Operation	V_{V1P5}	CL=1.1uF, IL=0mA	--	1.55	--	V
Line Regulation	--	CL=1.1uF, IL=0mA	--	--	10	mV
Support Current	--		--	--	30	mA
ADC Section (0V to 5V, 12-Bit, Single End Mode, Gain = 1) (Note5)						
ADC Input Voltage Range	V_{ADCIN}		0	--	V_{V5V}	V
Clock	f_{ADC_CLK}	ADC_CLK=SYSCLK/2	--	12	--	MHz
Conversion Rate	--	15T ADC CLK @12MHz	--	0.8	--	MSPS
Channel	--		--	8	--	
Current Limit Comparator Section (CMP0/CMP1/CMP2, CMP3 option) (Note5)						
Input Range	V_{IN}		0.1	--	V_{V5V}	V
Comparator Offset	V_{OFFSET}		-15	--	15	mV
Comparator Reference (8 levels)	V_{CMPREF}	CMPxN is selected as internal V_{CMPREF}	Typ. -20mV	0.125 0.250 0.375 0.500 0.625 0.750 0.875 1.000	Typ. +20mV	V
General Purposed Comparator (CMP2/CMP3/CMP4) (Note5)						
Input Range	V_{IN}		0	--	V_{V5V}	V
Comparator Offset	V_{OFFSET}		-15	--	15	mV
OPAMP (internal) (Note5)						
Input Range	V_{IN}		0	--	4.3	V
Output Range	--		0.05	--	4.95	V
Input Offset	V_{OFFSET}	Vout=2.5V	--	--	10	mV
Offset Bias Adjust	$V_{OFFBIAS}$	V_{V5V} = 5V	--	$V_{V5V}/2$ $V_{V5V}/40$	--	V
I/O of P0_0 to P0_7, P1_0 ~ P1_7, P2_0, P2_2, P2_4 section						
Input High Voltage	V_{IH}		--	--	0.7 x V_{V5V}	V
Input Low Voltage	V_{IL}		0.3 x V_{V5V}	--	--	V
Pull-Up Resistor	R_{PD}		20	--	100	kΩ
Pull-Down Resistor	R_{DOWN}		20	--	100	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V_{V5V}	--	15	--	mA
Low Level Output Current	I_{OL}	@ 0.2 x V_{V5V}	--	15	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
I/O of P2_1, P2_3, P2_5 section						
Input High Voltage	V_{IH}	Without internal Pull-up and Pull-down resistor	--	--	0.7 x V_{V5V}	V
Input Low Voltage	V_{IL}	Without internal Pull-up and Pull-down resistor	0.3 x V_{V5V}	--	--	V
Pull-Up Resistor	R_{PD}		20	--	100	kΩ
Pull-Down Resistor	R_{DOWN}		20	--	100	kΩ
High Level Output Current	I_{OH}	@ 0.8 x V_{V5V}	--	15	--	mA

Note 1: Absolute maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device out of its rated operating conditions.

Note 2: All voltages are with respect to the potential at the ground pin.

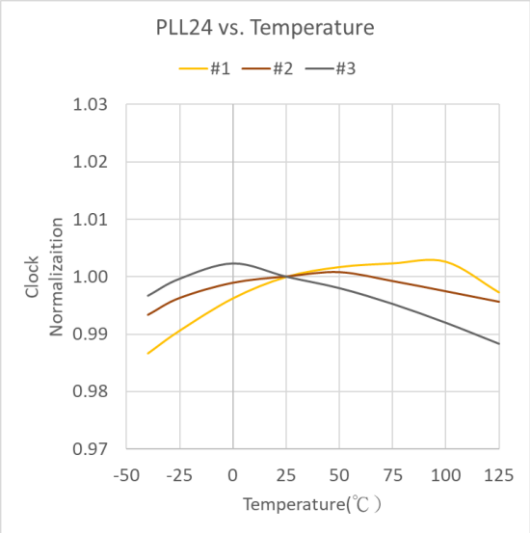
Note 3: Devices are ESD sensitive. Handling precaution is recommended.

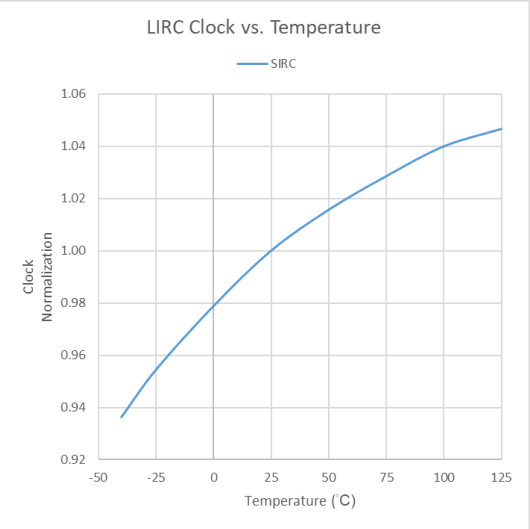
Note 4: Only default as 2.8V for LVR.

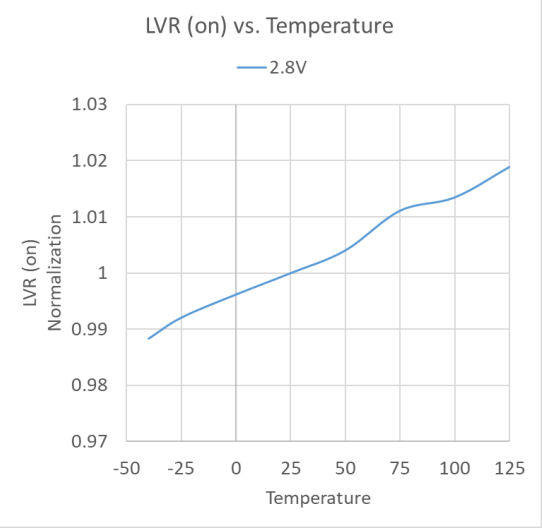
Note 5: Characterized, not tested at manufacturing.

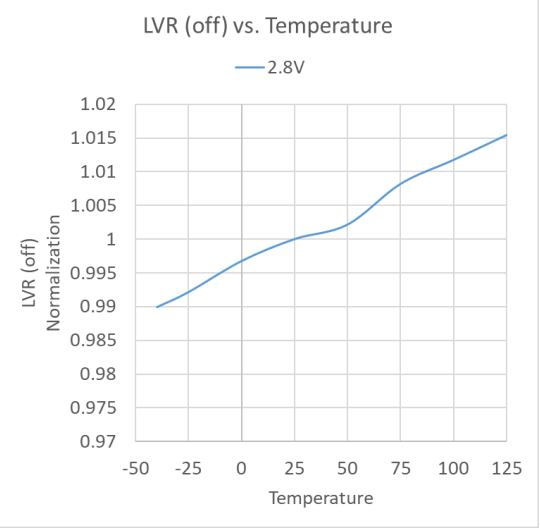
Note 6: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

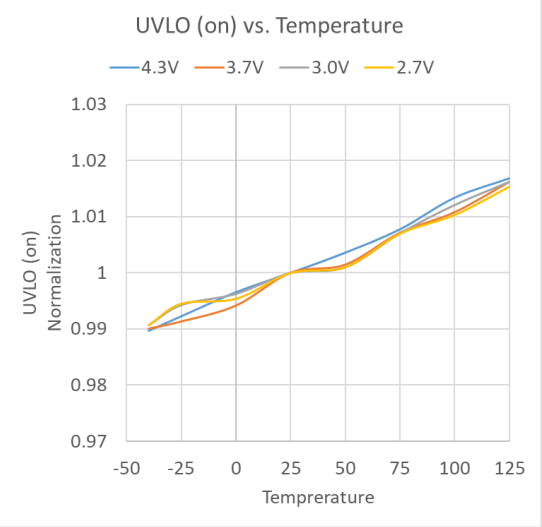
2.4. Typical Operating Characteristics

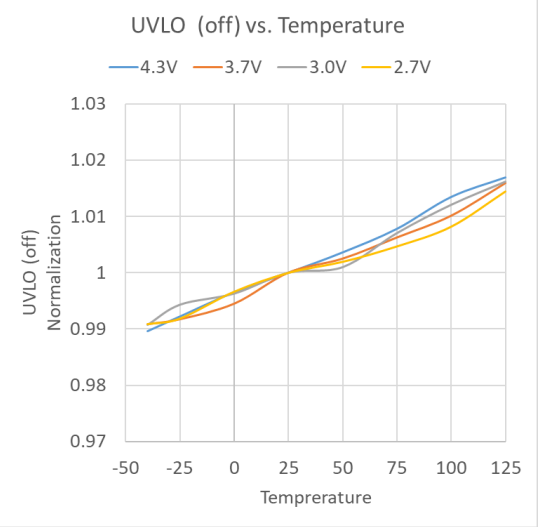












3. Device Description

3.1. Core

The core of the EMT1042 is the high-performance 8051 processor, and capable of running at speed up to 24MHz.

3.2. Flash and RAM

The EMT1042 embedded 32KB Flash program memory, 256B of IRAM, and 4KB of XRAM memory for storing user application code and data.

3.3. Code Protection

The EMT1042 provides users with the ability to enable flash protection to protect the code area. This can be enabled by call function from Library or the ESMT link tool.

3.4. Cyclic Redundancy Check (CRC)

CRC is a calculation method that divides this message polynomial by a constant called the generating polynomial. (the polynomial $F(x) = X^{16} + X^{12} + X^5 + 1$ given in ISO/IEC13239, CRC16-CCITT-False). It offers a mechanism only for validating storage errors in flash memory with CRC-16.

UART module provides an encoding mode and a check mode with CRC-8, and users can define the polynomial function.

3.5. Power Supply

The supply voltage V_{V5V} of EMT1042 ranges from 4.5V to 5.5V. All input/output (I/O) and internal voltage regulators are powered via the V_{V5V} pin externally.

3.6. LVR/POR/UVL

The EMT1042 integrates the Power-On Reset (POR) and Low-Voltage Reset (LVR) functions to ensure the system stability and initiates a reset when the voltage exceeds a threshold of 2.8V. Additionally, to prevent frequency reduction or erroneous data registration in low-voltage scenarios, the Under-Voltage Lockout (UVLO) feature employs programmable software to monitor voltage levels. It interrupts the system operation when the voltage drops below the preset threshold, providing the software with an opportunity to address the voltage anomaly.

3.7. Unique ID(UID)

The EMT1042 has an unique and read-only chip identification register that is a constant read from address 0xC818.

3.8. Vectored Interrupt Controller (VIC)

Interrupt source	Default Priority	Vector Address	Flag bit	Software Clear	Enable bit
Reset	Highest	0x0000	N/A	N/A	Keep on
PWM period interrupt [INT_PWM_RELOAD]	0	0x0003	IF0[0]	Y	IE0[0]
OCP detect, PWM braked interrupt [INT_PWM_BREAK] (**note1)**	1	0x000B	IF0[1]	Y	IE0[1]
$I_a/I_b/I_c$ phase current convert done interrupt [INT_ADC_CURRENT]	2	0x0013	IF0[2]	Y	IE0[2]
AD0~AD5 auto convert done interrupt [INT_ADC_SEQ] (**note2)**	3	0x001B	IF0[3]	Y	IE0[3]
INT_UART0_TX	4	0x0023	IF0[4]	Y	IE0[4]
INT_UART0_RX	5	0x002B	IF0[5]	Y	IE0[5]
TIMER0 interrupt [INT_TIMER0]	6	0x0033	IF0[6]	Y	IE0[6]
TIMER1 interrupt [INT_TIMER1]	7	0x003B	IF0[7]	Y	IE0[7]
CMP3 interrupt [INT_CMP3]	8	0x0043	IF1[0]	Y	IE1[0]
CMP4 interrupt [INT_CMP4]	9	0x004B	IF1[1]	Y	IE1[1]
Capture Module interrupt [INT_CAPTURE_PULSE]	10	0x0053	IF1[2]	Y	IE1[2]
Reserved	11	0x005B	IF1[3]	Y	IE1[3]
Under Voltage Lock-out interrupt [INT_UVL_ACTIVE]	12	0x0063	IF1[4]	Y	IE1[4]
Reserved	13	0x006B	IF1[5]	Y	IE1[5]
Reserved	14	0x0073	IF1[6]	N/A	IE1[6]
Reserved	15	0x007B	IF1[7]	N/A	IE1[7]

The EMT1042 provides 12 interrupt sources as shown in the table above. In this table, lower priority number indicates higher priority.

Note1: S/W Coil OCP protected event or H/W shunt OCP protected event.

Note2: Only one channel converted in one PWM period.

3.9. System Reset

The EMT1042 has 5 reset sources: external reset (RSTN), low-voltage reset (LVR), power-on reset (POR), under-voltage lockout reset (UVLR), and watchdog timer reset (WDT). Reset enable references related configuration registers, where the EN_AUVLRST and WDT_ON control bits respectively enable the UVLR and WDT reset sources.

3.10. Clock

- 12MHz internal High RC Oscillator (HIRC)
- 20~48KHz internal Slow RC Oscillator (SIRC)
- 24MHz internal PLL (PLL)

While system reset and startup, the internal High RC Oscillator is selected as default system clock.

3.11. Voltage Regulator

The voltage regulator powers the internal circuitry and the external VCAP capacitors are required.

3.12. Power Mode

The EMT1042 supports 2 working modes:

- Operation mode: the CPU core and peripheral modules continue to operate.
- Deep-sleep mode: the main clock is turned off. The CPU core is halted. The peripheral modules shall be powered down manually by selecting the appropriate function before entering deep sleep.

While in the Deep-sleep mode, the EMT1042 can be awakened via a specific pin. During normal operation, users have options to operate in different config based on user: such as turn off the clock, or power down the unused peripherals, allowing for flexible switching between power consumption and performance.

3.13. Universal Asynchronous Receiver/Transmitter (UART0)

The UART0 is a computer hardware device designed for asynchronous serial communication with configurable data format and transmission speed. It transmits data bit by bit individually, starts from the least significant bit(LSB) to the most significant bit(MSB), and be framed by a start and a stop bit to ensure precise timing management by the communication channel. The EMT1042 controller has one UART module (UART0).

- Half-Duplex/Full-Duplex support
- 40byte TX data buffers
- 40byte RX data buffers
- CRC-8 check support, and 0x00 or 0xFF as initial value
- Tx or Rx signal invert Support
- No parity bit support

3.14. Multiplication Division Unit (MDU)

The EMT1042 integrates a hardware multiplication and division unit(MDU). The MDU supports signed and unsigned four kinds of operations: 32bit x 32bit, 16bit x 16bit, 32bit / 16bit, and 16bit / 16bit. MDU can be either signed or unsigned. The mode of MDU can be selected by MD_MODE register.

3.15. Timers and Watchdog

The EMT1042 includes 2 basic timer and 1 watchdog timer.

Timer and Watchdogs								
Timer Type	**Name**	**Clock src**	**Counter**	**Pre-scaler**	**Counting Dir.**	**Interrupt**	**PWM**	**Capture Compare Channel**
Basic	Timer0	Sysclk	16 bits	8 bits	Inc.	Yes	No	No
Basic	Timer1	SIRC	8 bits	No	Inc.	Yes	No	No
Watchdog	WDT	Sysclk	16 bits	8 bits	Inc.	Yes	No	No

-Basic Timer (Timer0)

Timer0 is a 16-bit timer comprised of two 8-bit registers: T0_CNT_H (high byte) and T0_CNT_L (low byte). It operates in a flexible 16-bit auto-reload mode, utilizing two 8-bit registers: T0_PERIOD_H (high byte) and T0_PERIOD_L (low byte). Timer0 can be clocked by the system clock and divided by an 8-bit pre-scaler: T0_PRESCALE.

-Basic Timer (Timer1)

Timer1 is a 8-bit timer comprised of an 8-bit register: T1_CNT. It operates in a flexible 8-bit auto-reload mode, utilizing an 8-bit register: T1_PERIOD.

-Watchdog Timer (WDT)

The WDT is a 16-bit up counter driven by the WDT_CLK. The WDT_CLK operates independently of the main clock, and continues counting even in shutdown and standby modes. This watchdog can function as a safety mechanism to reset the device in case of CPU malfunctions, or function as a free-running timer for timeout management.

WDT_CLK = SYS_CLK/(4n+1), n=0~255

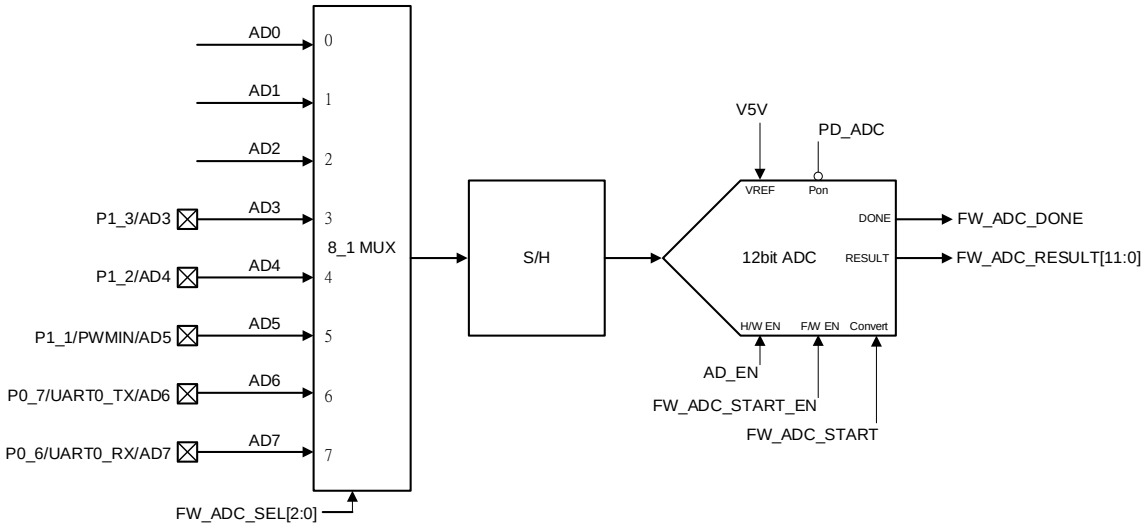
3.16. General Purpose Input/Output (GPIO)

1. The P0[7:0], P1[7:0], and P2[5:0] registers are mapping to I/O pins P0_0~P0_7, P1_0~P1_7, and P2_0~P2_5 respectively.
2. PORT0_OE, PORT1_OE, and PORT2_OE registers are used to configure the logic output enable settings of P0_0~P0_7, P1_0~P1_7, and P2_0~P2_5. However, for P2_1, P2_3, and P2_5, if set as output enable, they support source output function only and cannot support sink output.
3. PORT0_OD, PORT1_OD, and PORT2_OD registers are used to configure the output open-drain mode for P0_0~P0_7, P1_0~P1_7, and P2_0, P2_2, P2_4. By default, they operate in push-pull mode. For P2_1, P2_3, and P2_5 pins, there are no output open-drain mode.
4. PORT0_IE, PORT1_IE, and PORT2_IE registers are used to configure the logic input enable settings for P0_0~P0_7, P1_0~P1_7, and P2_0~P2_5. By default, they are enabled.
5. All ports can be enabled weak pull-up via PORT0_PU, PORT1_PU and PORT2_PU.
6. All ports can be enabled weak pull-down via PORT0_PD, PORT1_PD, and PORT2_PD. Upon system startup, weak pull-down is the default setting.
7. P0_6, P0_7, P1_0~P1_7, and P2_0~P2_5 pins are multi-function pins with analog input of ADC, OPAMP, and comparator. Each analog module has an Enable register to enable the function or not.
8. The PWM_HL_EN register controls the three-phase outputs AH/BH/CH and AL/BL/CL. These outputs are from P0_0 to P0_5.

3.17. Analog to Digital Converter (ADC)

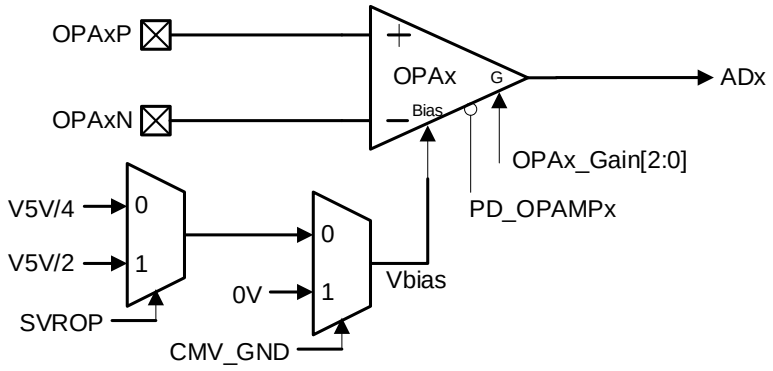
In the EMT1042, there is a 12-bit 8 channels SAR ADC. AD0/AD1/AD2 are connected to the outputs of internal operational amplifiers.

- For software ADC sampling, FW_ADC_START_EN must be set to 1.
- Set the FW_ADC_START_EN bit to 1 to launch one time of ADC sampling and conversion. Once the conversion is done, the FW_ADC_START_EN bit will be cleared automatically.
- Set the FW_ADC_START to 1 to initiate continuous ADC sampling and conversion.
- Configure the FW_ADC_SEL[2:0] to select different input channels for sampling. The ADC result is stored in the FW_ADC_RESULT[11:0] after each AD conversion.
- 15 ADC_CLK is needed for each ADC sampling conversion. (15T ADC_CLK = 30T SYS_CLK, system clock)
- When the SVM Mode function is activated, it is important to set the FW_ADC_START_EN bit to 0 to prevent interference with the real-time automatic trigger mode of the internal circuitry, especially during the motor drive timing sequences operation.



3.18. OPAMP(OPA)

The EMT1042 has 3 independent operational amplifiers, OPA0, OPA1, and OPA2. Each OPA has its own power-down bit, PD_OPAMPx. PD_OPAMPx=1 indicates that the OPAx is powered down, oppositely setting it to 0 indicates that the OPAx is powered on. The same bias voltage (Vbias) for all OPAs can be selected as 0V, V5V/4, or V5V/2 by configuring the settings of CMV_GND and SRVOP.



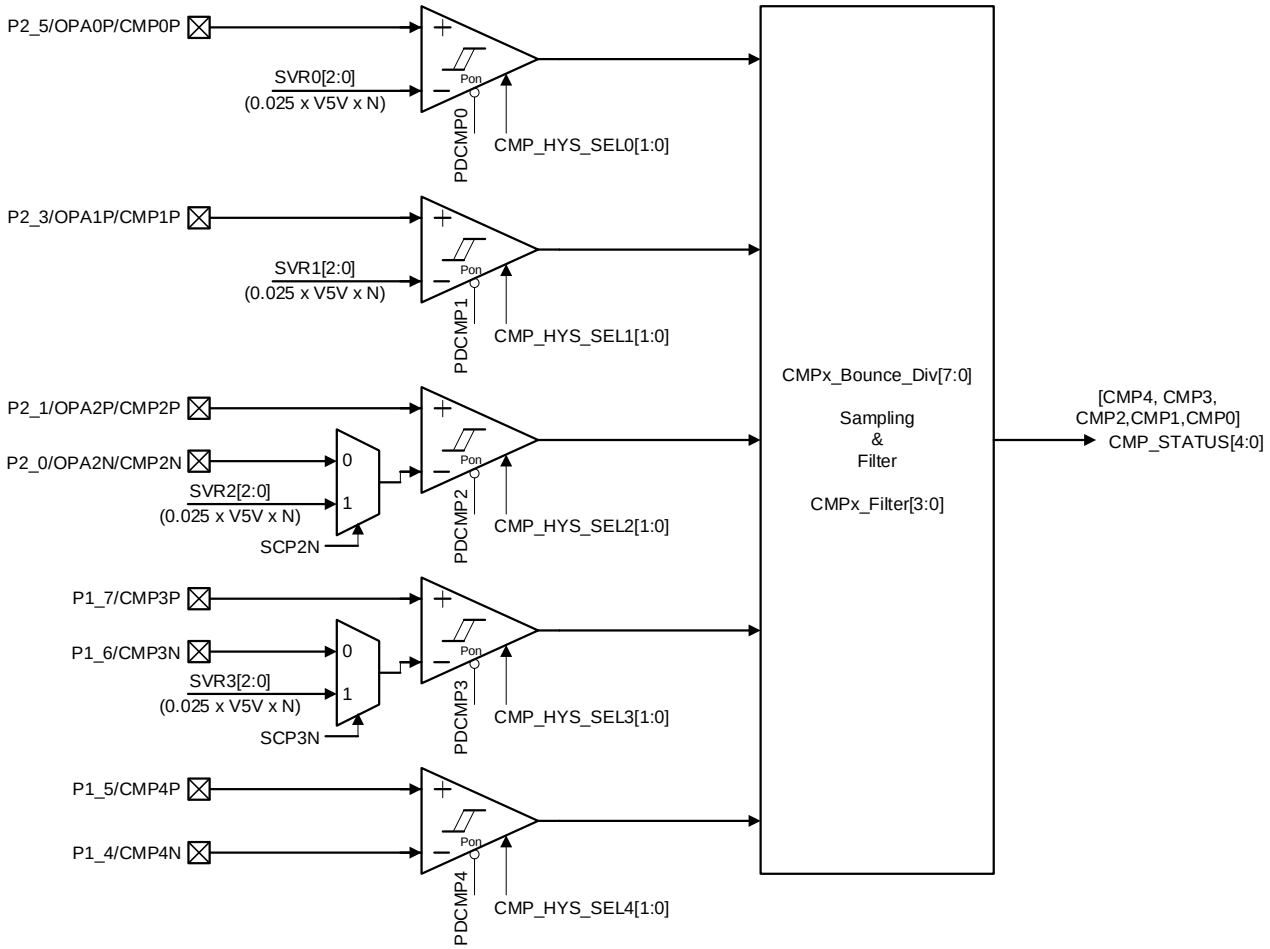
The output (Vo) of the operational amplifier is connected to the ADx interface internaly(?) and given by Vo = Vin × Gain + Vbias.

3.19. Comparator (CMP)

The EMT1042 provides 5 independent analog comparators. Three of them (CMP0/CMP1/CMP2) are primarily used for over-current sensing. CMP3 and CMP4 are primarily used for Back-EMF feedback and speed detection. Each comparator has its own power-down bit, PDCMPx. PDCMPx=1 indicates that the comparator is powered down, oppositely setting it to 0 indicates that the comparator is powered on.

Additionally, the sampling division (CMPx_Bounce_Div) and digital signal filtering (CMPx_Filter) functions are available. (Noted: When using the CMP module, it is important to set HW_EN=1 to enable the module.)

CMP2 and CMP3 have either the configurable internal reference voltage or the external input. CMP0/CMP1/CMP2/CMP4 have configurable negative inputs as internal reference configurable voltage.



3.20. PWMIN(h_SPD)

The duty cycle comparator input is connected to a specific pin, PWMIN. The frequency range of PWM input signal for detection is 1k to 100kHz. Duty cycle result(0 to 4095) is obtained from the combination of two 8-bit registers: h_SPD_H (high byte) and h_SPD_L (low byte).

3.21. CAPTURE(CAP)

The capture module operates with an 8MHz clock source. It's responsible for measuring the durations of both the pulse high and pulse low signals.

- The pulse high duration is recorded using three 8-bit registers: Positive_Pulse_H (high byte), Positive_Pulse_M (middle byte), and Positive_Pulse_L (low byte).
- Similarly, the pulse low duration is captured with three 8-bit registers: Negative_Pulse_H (high byte), Negative_Pulse_M (middle byte), and Negative_Pulse_L (low byte).

3.22. Pulse Width Modulation (PWM)

The motor control Pulse width modulated (PWM) output on its specific-pin. The frequency of the output is dependent on the time base for the PWM_CNT, and the setting of the PWM cycle length (16-bits). It is important to note that all channels configured for 16-bit PWM mode will use the same cycle length. It is not possible to configure one channel for different cycle length. However, the PWM timer composed of two 8-bit registers: PWM_CNT_H (high byte) and PWM_CNT_L (low byte). PWM timer may be clocked by the system clock. The cycle length composed of two 8-bit registers: REG_PWM_PRD_H (high byte) and REG_PWM_PRD_L (low byte).

3.23. Digital to Analogs (PWM_DAC)

EMT1042 provides a digital DAC out module, the frequency is the same as PWM carrier frequency. Writing a 16-bit value to the PWM_DA register to change the duty. PWM_DA is formed of 8-bit registers.

$$Duty = \frac{REG\_PWM\_PRD - PWM\_DA}{REG\_PWM\_PRD}$$

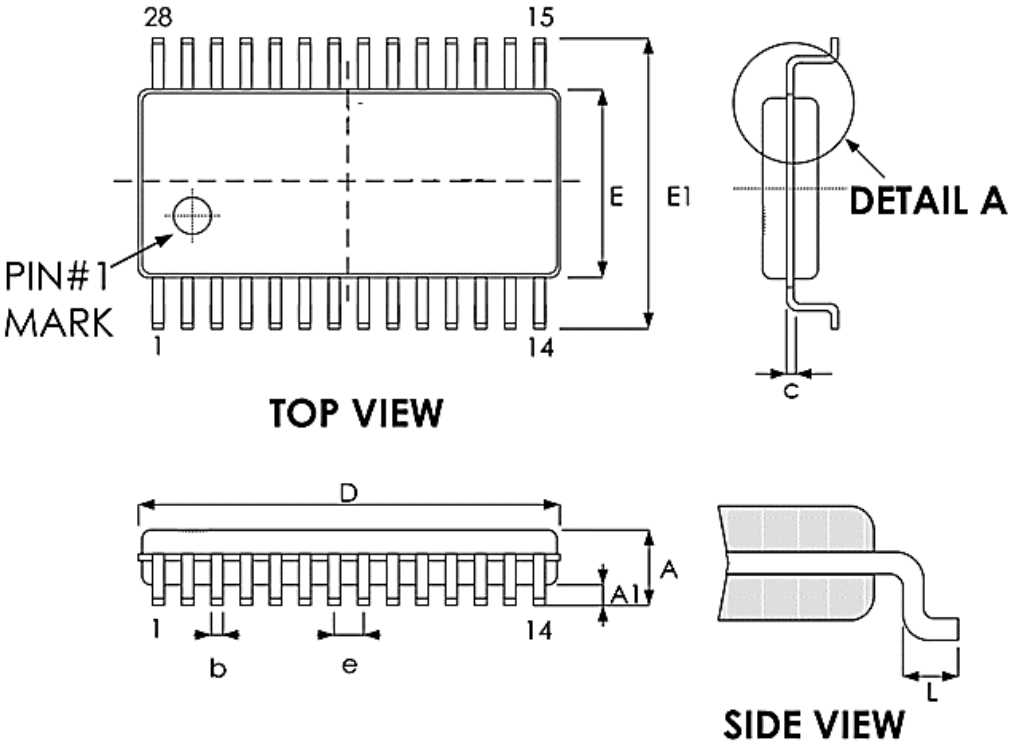
3.24. Motor Arithmetic Unit (MAU)

EMT1042 provided a sine-wave motor control method with a built-in SVPWM digital circuit to drive a BLDC motor. This MAU also supported the sensorless and Hall ICs driving algorithm to control the BLDC motor rotating smoothly. In order to cover the complex BLDC application and motor driving situation this MAU integrated many digital circuit modules about the motor driving algorithm shown as below.

1. Speed loop PID module,
2. current zero crossing detection module,
3. Initial position detection module,
4. SVPWM module,
5. Phase adjusting module,
6. ADC LPF module,
7. High PWM resolution algorithm module,
8. Voltage feedforward compensation module,
9. Hall sensor speed and back EMF speed calculation module

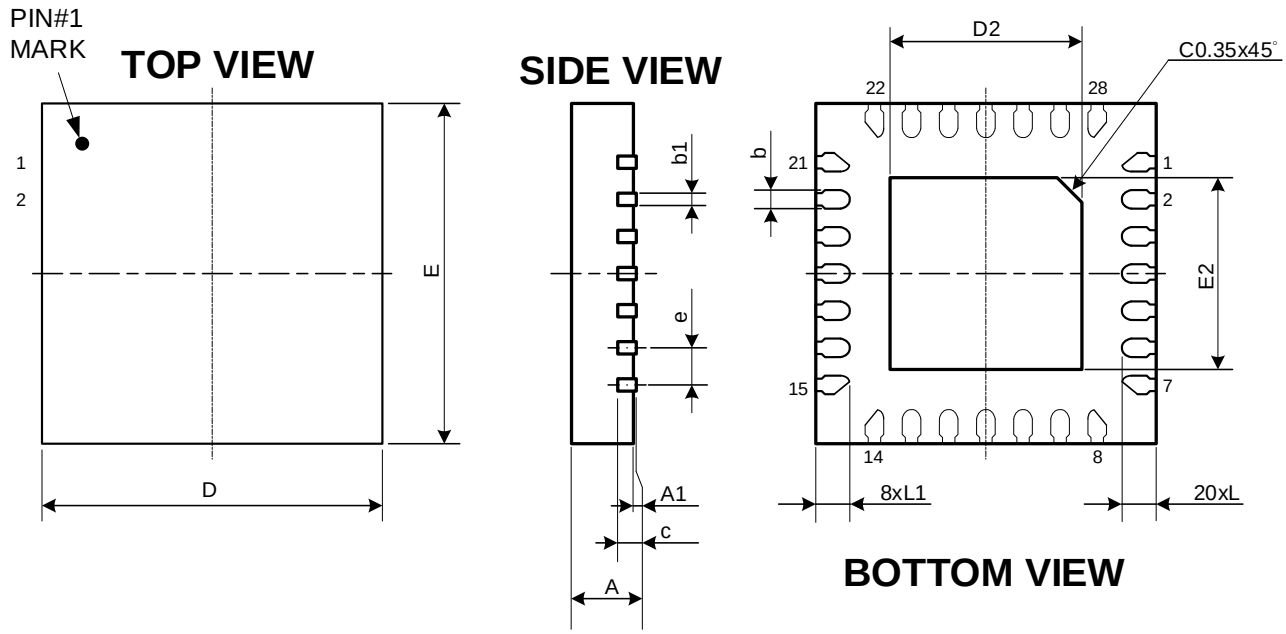
4. Package Outline Drawing

TSSOP-28L (173 mil)



Symbol	Dimension in mm	
	Min.	Max.
A	--	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	9.60	9.80
E	4.30	4.50
E1	6.30	6.50
e	0.65 BSC	
L	0.45	0.75

TQFN4x4-28L (Pitch:0.45mm)



Symbol	Dimension in mm	
	Min.	Max.
A	0.70	0.80
A1	0.00	0.05
b	0.15	0.25
b1	0.14REF	
c	0.18	0.25
D	3.90	4.10
E	3.90	4.10
e	0.45 BSC	
L	0.35	0.45
L1	0.31	0.41

Exposed pad

Symbol	Dimension in mm	
	Min.	Max.
D2	2.30	2.50
E2	2.30	2.50

5. Revision History

Revision	Date	Description
1.0	2024.12.27	Original

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